IN THE CLAIMS

We claim:

1. A process, comprising:

providing a substrate;

etching at least one trench into the substrate, the at least one trench having a pair of walls and a bottom;

forming a first electrode within the trench over the pair of walls and the bottom; and

forming a second electrode within the trench over the pair of walls and the bottom.

2. The process of claim 1, wherein the first electrode is parallel to the second electrode.

3. The process of claim 1, wherein the at least one trench has a length and a width and wherein the first electrode and the second electrode are at approximately a 90° angle to the length of the at least one trench

4. The process of claim 1, further comprising forming an insulator liner layer above the semiconductor substrate before forming the first and second electrodes.

5. The process of claim 4, wherein forming an insulator liner layer comprises:

depositing a silicon nitride layer;

depositing a polysilicon layer above the silicon nitride layer; and

oxidizing the polysilicon layer to form a silicon oxide layer.

6. The process of claim 1, wherein forming the first electrode and forming the second electrode comprises:

depositing a conductive layer within the at least one trench over the pair of walls and the bottom;

patterning a resist above the conductive layer; and

etching the conductive layer.

7. The process of claim 6, further comprising depositing a sacrificial light absorbing material comprising SLAM™ above the conductive layer before patterning the resist above the conductive layer.

8. The process of claim 1, wherein etching an at least one trench comprises etching a plurality of trenches and a plurality of rows of the plurality of trenches into the substrate.

9. The process of claim 1, wherein the substrate is a silicon die.

10. The process of claim 1, wherein the first electrode and the second electrode are platinum.

11. A process, comprising:

etching a plurality of parallel trenches into a silicon substrate, the trenches each having a contour of a pair of walls and a bottom;

forming an oxide liner layer along the contour of the trenches;

depositing a platinum film over the oxide liner layer along the contour of the trenches;

patterning the platinum film, wherein patterning the platinum film comprises depositing a sacrificial light absorbing material comprising SLAM™ above the platinum

film, patterning a resist above the SLAM™, and etching the SLAM™ not covered by the resist; and

etching the platinum film with an isotropic etch to form a pair of electrodes over the contour of the trenches.

12. The process of claim 11, wherein trenches are separated by a distance in an approximate range of 5um to 50um.

13. The process of claim 11, wherein the plurality of parallel trenches each have a high aspect ratio of height to width in the approximate range of 10:1 and 100:1.

14. A process, comprising:

providing a trench having a pair of walls and a bottom, the trench having a first electrode formed within the trench over a portion of the pair of walls and the bottom of the trench and a second electrode formed within the trench over a portion of the pair of walls and the bottom of the trench, the second electrode separate from the first electrode by a distance; and

maximizing a flow rate of a liquid in the trench by increasing an electric field created by the first electrode and the second electrode across the trench by minimizing the distance between the first electrode and the second electrode.

15. The process of claim 14, wherein the flow rate is in the approximate range of 1 ml/s and 50 ml/s.

16. The process of claim 14, further comprising applying a voltage to the first electrode, and wherein the second electrode is grounded.

17. A device, comprising:

an at least one trench etched in a substrate, the at least one trench having a pair of walls and a bottom;

a first electrode formed within the at least one trench over a portion of the pair of walls and the bottom; and

a second electrode formed within the at least one trench over a portion of the pair of walls and the bottom, the second electrode parallel to, but separate from, the first electrode.

18. The device of claim 17, wherein the substrate has a plurality of active semiconductor devices formed on a side opposite to the at least one trench and the first and second electrodes.

19. The device of claim 17, wherein the at least one trench has a length in an approximate range of 10um and 500um.

20. The device of claim 17, wherein the at least one trench has a depth in an approximate range of 5um to 200um.

21. The device of claim 17, wherein the at least one trench has a width in an approximate range of 1um to 500um.

22. The device of claim 17, wherein the at least one trench comprises a plurality of trenches and a plurality rows of the trenches.

23. The device of claim 22, wherein the plurality of rows comprises between approximately 20 rows to approximately 1000 rows.

24. The device of claim 22, wherein the number of trenches per row is in an approximate range of 100 trenches to 2000 trenches.

25. The device of claim 17, wherein the first electrode and the second electrode are platinum.

26. The device of claim 17, further comprising an insulating liner material in between the at least one trench and the first and second conductive lines formed above the at least one trench.

27. The device of claim 26, wherein the insulating liner comprises a layer of silicon nitride formed above the substrate and a layer of silicon dioxide formed above the layer of silicon nitride.

28. A microelectronic package, comprising:

a substrate having at least one electroosmotic pump comprising a trench and a first electrode and a second electrode formed within the trench;

a radiator.

29. The microelectronic package of claim 28, wherein the substrate is a silicon die comprising a first side on which the at least one electroosmotic pump is formed, and a second side wherein semiconductor devices are formed.

30. The microelectronic package of claim 28, wherein the substrate is a heat management substrate coupled to a die on which semiconductor devices are formed.